UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,494	12/28/2005	Peter Joest	10191/4190	2456

26646 7590 05/14/2010

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
MITCHELL, JASON D	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
05/14/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/539,494	JOEST, PETER	
	Examiner	Art Unit	
	Jason Mitchell	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/17/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on 2/12/10.

Claims 19-37 are pending in this application.

Response to Arguments

Information Disclosure Statement

The copies of "Maintainable ROS Code Through the Combination of ROM and EEPROM"" and GB 2 373 888 have been received and considered.

Rejection of Claims 29 and 31 under 35 USC 112 1st & 2nd

The applicant's amendments are sufficient to overcome the previous rejection of claims 29 and 31 under 35 USC 112 which are consequently withdrawn.

Rejection of Claim 36 under 35 USC 101

The applicant's amendments are sufficient to overcome the previous rejection of claim 36 under 35 USC 101 which is consequently withdrawn.

Rejection of Claims 19-26, 30 and 34-36 under 35 USC 102(e)

In the last par. on pg. 9, the applicant states:

> Ren refers to a method of updating software in which the software is first divided into sections (col. 4, lines 50-60). An Update-Processing-Routine is added to each section to check for software updates whenever each section is executed (col. 5, lines 22-25; Fig. 4). Unlike the subject matter of claim 19 (in which a branching to the second memory area is automatically performed when the exit address portion of the first memory area is reached), Ren requires the addition of software routines, i.e.,

> the Update-Processing-Routine, to check for updates before determining whether to jump to a patched software section. Even when a so-called "direct jump" (col. 7, lines 33-40; Fig. 5) is used, a software routine is required to be executed in order to determine whether to make the jump. Therefore, Ren does not disclose or suggest "overwriting at least a portion of the old software parts with an exit address that causes the performance of a first branching from the first memory area to a location in the new software parts whenever the overwritten portion is reached during execution of a corresponding old software part," as recited in claim 19.

The examiner respectfully disagrees. In addition to overwriting a portion of the old software to direct execution to an Update-Processing-Routine to determine the existence and address of a patch routine (e.g. col. 7, lines 12-18) Ren also discloses an embodiment where a portion of the old software parts is overwritten with an address of the patch routine (e.g. col. 8, lines 43-48 “When there is a corresponding patch programmed in the patch area … the first and the only instruction of the Update-Processing-Routine will be changed so that the CPU/DSP execution will be directed to the … start address of patch program”). Accordingly, the applicant’s arguments are not persuasive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-26, 30 and 34-36 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,760,908 to Ren (Ren).

Regarding Claims 19 and 34-36: Ren discloses a method for changing software in a first memory area in a control unit for controlling operational sequences, the method comprising:

replacing execution of old software parts with execution of new software parts (col. 5, lines 5-6 "The software patch is then used for execution instead of using the program codes in S2."); and

overwriting at least a portion of the old software parts with an exit address that causes the performance of a first branching from the first memory area to a location in the new software parts whenever the overwritten portion is reached during execution of a corresponding old software part (col. 8, lines 43-48 "When there is a corresponding patch programmed in the patch area … the first and the only instruction of the Update-Processing-Routine will be changed so that the CPU/DSP execution will be directed to the … start address of patch program");

wherein the old software parts are written into the first memory area (col. 4, lines 8-10 "A software program resides in FLASH/ROM memory 115"), the new software parts are written into a second memory area (col. 4, lines 37-40 "writing patch data into the patch database 310") and, due to the first branching (col. 5, lines 48-53 "directs CPU/DSP execution to jump 506 to the start address 502 of patch program 507"), instead of the old software parts being executed in the first memory area, the new

software parts are executed in the second memory area (col. 5, lines 5-6 “The software patch is then used for execution instead of using the program codes in S2.”), the control unit, following the execution of the new software parts, branching back again into the first memory area via a second branching in the second memory area and the execution of the other software distinct from the old software parts being continued in the first memory area, the old software parts remaining, at least in part, unmodified in the first memory area (col. 5, lines 55-59 “After executing the patch program 507 … jump 508 to a predetermined place in the original software”; note that only the Jump instruction (see col. 8, 55-60) has been changed).

Regarding Claim 20: The rejection of claim 19 is incorporated; further Ren discloses the second memory area is only used to receive the new software parts (col. 4, lines 37-40 “the patch database 310”).

Regarding Claim 21: The rejection of claim 19 is incorporated; further Ren discloses the first branching and the second branching are implemented by at least one chained list (col. 6, lines 25-30 “using an intermediate step, such as the Patch_Control_Routine 609, for directing CPU/DSP instruction pointer to jump to the start address 602 of patch program 607”).

Regarding Claim 22: The rejection of claim 19 is incorporated; further Ren discloses as a first branching a start address of the new software parts is used, this being used to

overwrite at least partially the old software parts (col. 8, lines 43-48 “instruction of the Update-Processing-Routine will be changed, so that the CPU/DSP execution will be directed to the start address of the ... patch program").

Regarding Claim 23: The rejection of claim 19 is incorporated; further Ren discloses as the second branching a start address of the additional software distinct form the old software parts is used (col. 5, lines 55-59 “After executing the patch program 507 … jump 508 to a predetermined place in the original software”).

Regarding Claim 24: The rejection of claim 19 is incorporated; further Ren discloses the new software parts contain information that indicate which old software parts are to be replaced (col. 18, lines 26-27 “Software Section Identifiers of the software sections that are updated by this patch”).

Regarding Claim 25: The rejection of claim 19 is incorporated; further Ren discloses the new software parts contain information that indicate by which new software parts the old software parts are to be replaced (col. 18, lines 12-15 “Address information of patch data”).

Regarding Claim 26: The rejection of claim 19 is incorporated; further Ren discloses the second memory area, in addition to at least one new software part (col. 8, lines 16-17 "Patch program codes”), contains an address for the first branching (col. 18, lines 55-

63 "The patch program contains … a Patch Start Address"), an address for the second branching (col. 18, lines 55-63 "The patch program contains … an instruction for jumping back to a predetermined place in the embedded software") and an address for the start of the old software part, which is to be replaced by the at least one new software part (col. 18, lines 26-27 "Software Section Identifiers of the software sections that are updated by this patch").

Regarding Claim 30: The rejection of claim 19 is incorporated; further Ren discloses as the first memory area a first table and as the second memory area a second table are provided in the same memory (col. 6, lines 41-43 "Memory area for containing patch program codes can be allocated … at a place inside of the embedded software code area").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27-29 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,760,908 to Ren (Ren) in view of US 6,076,134 to Nagae (Nagae).

Regarding Claim 27: The rejection of claim 26 is incorporated; further Ren does not disclose the second memory area furthermore contains the length of at least one of the at least one new software part and of the at least one old software part.

Nagae teaches a second memory area furthermore contains the length of at least one of the at least one new software part and of the at least one old software part (col. 4, lines 8-13 “The patch table 21 comprises … data length DL").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include length data in Ren’s patch table (col. 4, lines 37-40 “writing patch data into the patch database 310”) as taught by Nagae (col. 4, lines 8-13 “The patch table 21 comprises … data length DL"). Those of ordinary skill in the art would have been motivated to do so as a known alternate implementation which would have provided the additional benefit of eased access to the patch data (Ren col. 5, lines 13-22 “Size of a software section may not be a fixed number … can be based on … number of lines of program lines”’; col. 18, lines 28-29 “Other information to describe patch program and data area update”; Nagae col. 4, lines 8-13 “The patch table 21 comprises variable length records”).

Regarding Claim 28: The rejection of claim 27 is incorporated; further Ren discloses the addresses are integrated into a data record in the second memory area (col. 18, lines 12-15 “Address information of patch data”).

Regarding Claim 29: The rejection of claim 28 is incorporated; further Ren discloses at least two old software parts and the at least two new software parts, which replace these, are provided (col. 6, lines 15-18 "a list of identifiers of the patches"; discloses plural patches), and the data record is created and stored in the second memory area for each instance of an old software part having a corresponding new software part (col. 18, lines 12-15 “address information of patch data”; col. 4, lines 37-40 “writing patch data into the patch database 310”).

Regarding Claim 32: The rejection of claim 28 is incorporated; further Ren discloses every data record or every software section is provided with an identification (col. 4, lines 55-57 “The locations can be expressed by L1, L2, …, Ln, in the order from small address to large address”).

Regarding Claim 33: The rejection of claim 32 is incorporated; further Ren does not disclose the identification for a software section in the first memory area, which contains an old software part, and the identification for the corresponding software section having the new software part, which replaces the old software part, are the same.

Nagae teaches patch data wherein the identification for an old software section and the identification of a new software section are the same (e.g. Fig. 3, col. 212 “ID”; col. 4,

24-28 “Each identifier ID in column 212 … includes an identification code for identifying an object program to be patched").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same identifier (Nagae col. 4, 24-28 “Each identifier ID in column 212 … includes an identification code for identifying an object program to be patched") in Ren’s patch data (col. 20, lines 14-16 “The patch identification information may include … Patch Identifier, and software section identifier”). Those of ordinary skill in the art would have been motivated to do so and an alternate implementation which would, at least, reduce the size of the patch table and indicated the necessary correspondence between patches and software sections (col. 6, lines 14-19 “a list of identifiers of the patches … and/or a list of the corresponding identifiers of the software sections”).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,760,908 to Ren (Ren) in view of US 5,802,549 to Goyal et al. (Goyal).

Regarding Claim 31: The rejection of claim 19 is incorporated; further Ren does not disclose the first memory area and the second memory area are each divided into software sections, a size of the software section of the first memory area being equal to a size of the software section of the second memory area, a new software part being written into each software section of the second memory area.

Goyal teaches a first and second memory area are each divided into software sections, a size of the software section of the first memory area being equal to a size of the software section of the second memory area and patches are applied to whole sections (col. 1, lines 43-48 “For each page of ROM to be updated, i.e., patched, a page in RAM is reserved").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to divide Ren’s first and second memory areas (Fig. 2, RAM 240 & FLASH/ROM 245) into uniform sections (Goyal col. 1, lines 43-48 “page of ROM … page in RAM”) wherein patching the old software comprises patching an entire section (Goyal col. 1, lines 46-49 “the reserved RAM page is read instead of the corresponding ROM page”). Those of ordinary skill in the art would have been motivated to do so as a known alternative method of implementing the functionality disclosed by Ren which would only produce the expected results (col. 5, lines 13-22 “Determining locations of L1, L2, …, Ln and partitioning embedded software into software sections ... can be based on ... hardware design schemes … as can be appreciated by those skilled in the art").

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,760,908 to Ren (Ren) in view of US 6,076,134 to Nagae (Nagae) in view of US 2005/0257208 to Blumfield et al. (Blumfield).

Regarding Claim 37: The rejection of claim 28 is incorporated; further Ren discloses restoring full execution of the old software parts (col. 8, lines 38-42 “When there is no corresponding patch programmed in the patch area … the first and the only instruction of the Update-Processing-Routine is to JUMP to Label_O, which is the start address of the original code") and modifying the old software parts to reflect the contents of the second memory area (col. 8, lines 38-42 “When there is no corresponding patch … JUMP to Label_O "; col. 8, lines 43-48 “When there is a corresponding patch … execution will be directed to the … start address of patch program”).

Ren and Nagae do not explicitly teach full execution of the software parts is restored by deleting the data record.

Blumfield teaches restoring full execution of old software parts by deleting a patch data record (par. [0025] "permit the patch to be quickly disabled by simply deleting the patch from the set of patches").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to automatically restore full execution of the old software parts (Ren col. 8, lines 38-42 “Jump to Label_O”) in response to deleting the data record (Ren col. 8, lines 43-48 “patch program”; Blumfield par. [0025] "deleting the patch from the set of patches"). Those of ordinary skill in the art would have been motivated to do so as a known and implementable means of ‘uninstalling’ a patch which would have produced

only the expected results and would have “permit[ed] a patch to be quickly disabled ... if it is discovered that the patch is creating problems" (Blumfield par. [0025])

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Mitchell whose telephone number is (571)272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Bullock Lewis can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason Mitchell/
Primary Examiner, Art Unit 2193